Design and Modeling of a High-Q On-Chip Hairpin Inductor for RFIC Applications

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Abstract *— The design and modeling of a high Q hairpin inductor is presented. The inductor is designed and fabricated using the thick top-level metal (4um thickness, 14um away from the substrate) in an IBM 0.5um SiGe BiCMOS process to provide very high peak Q, approaching 27 from 2 to 4GHz, specifically for integrated voltage-controlled-oscillator (VCO) applications. A broadband lumped-element model is also developed for this structure. The modeling methodology is verified using commercial field solvers (IE3D and ADS Momentum) and hardware measured data, the results show that the derived model is correlates with the EM simulation data.*

I. INTRODUCTION

Building high-quality on-chip inductors has attracted tremendous interest from the RFIC design community and semiconductor manufacturers [1-3]. High-quality on-chip inductors have been widely demonstrated as a key factor for successfully integrating RF building blocks, such as voltage-controlled oscillator (VCO's). The on-chip inductor quality factor will directly affect the phase noise of an integrated VCO [3]. In order to improve the quality factor (Q) of the integrated inductors, semiconductor manufactures have designed many process variations, such as increasing metal thickness and the distance of the metal to the lossy substrate and adding a second Cu metal layer to form a dual metal inductor to further increase the metal thickness and thus improve the inductor Q [4].

This paper presents a high Q on-chip "hairpin" inductor design and its efficient modeling technique. The high Q is achieved by optimizing the width of the conductor to increase the surface area for current flow. The inductor and its Q are optimized for on-chip VCO designs at 2~5GHz. The computational modeling approach generates a lumped-element model, which can be easily used in RFIC design simulations. The accuracy of the model has been verified through EM simulations.

II. HIGH Q INDUCTOR IN VCOs

In an integrated LC-tank VCO design, an active network with negative transconductance, $-G_M$, is connected to the LC resonator with an equivalent parallel resistance, Rp. The negative resistance (-1/GM) provided from the active circuit is used to compensate the tank loss due to Rp, so that an undamped oscillation can be sustained. The Q of the resonator circuit has been shown to be an important parameter directly related to the phase noise of a VCO [5]:

$$S(\Delta\omega) \cong \left[\frac{2FKT}{P_s}\right]\cdot\left[1+\frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right]\cdot\left[1+\frac{\omega_c}{\Delta\omega}\right] \quad (1)$$

where $S(\Delta\omega)$ is the single-sideband output power spectral density of the phase noise at an offset frequency $\Delta\omega$ from the oscillation frequency ω_0, Q is the tank loaded quality factor, which includes all the loading losses. P_s is the power of the signal, F is a factor that is related to the noise introduced by the active circuit, ω_c is the corner frequency which is the frequency where $S(\Delta\omega)$ changes from $1/(\Delta\omega)^2$ curve to $1/(\Delta\omega)^3$ curve. From (1), it is clear that increasing the tank Q is an effective way to improve the phase noise of a VCO circuit. The loaded Q of an LC resonator is usually dominated by the inductor Q, since the on-chip capacitor usually has very high Q in most of the processes [6].

III. INTEGRATED HAIRPIN INDUCTORS

Many efforts have been focused on optimizing the processes to realize high quality integrated inductors with the least additional process complexity. IBM SiGe BiCMOS and RFCMOS processes utilize an enhancement to the traditional back-end-of-line (BEOL) process to improve the inductor Q [4]. These processes consist of a resistive substrate (11-16 Ohm-cm), a 4um thick metal layer, and a thick oxide dielectric (14um) between this metal layer and the substrate. The optimum strategy here is to minimize the conductor loss and the parasitic capacitance to the substrate so that the inductor Q can be improved. The hairpin inductor is designed based on all these beneficial features of the technology and at the same time, optimizing the width of the conductor to further increase the surface area for current follow so that the current crowding loss due to the skin effect is minimized. The hairpin inductor layout, designed in an IBM 0.5um SiGe BiCMOS process, is shown in Figure 1.

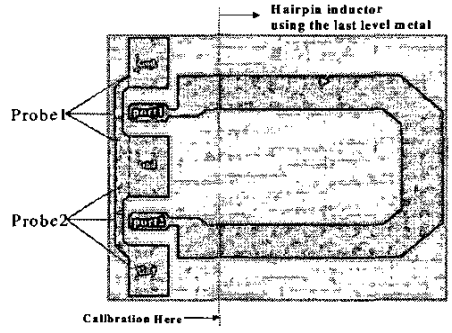

Figure 1. Layout of hairpin inductor.

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IV. CIRCUIT MODEL EXTRACTION

In this section, we describe the modeling approach for the Hairpin inductors.

A. *Traditional Approach*

A general equivalent pi-circuit for an integrated inductor is shown in Figure 2. The resistance R models the conductor loss and the skin-effect loss, R_{sub} models the substrate loss and the loss due to eddy currents induced inside the substrate. C_F models the turn to turn capacitance of a spiral inductor and C_{OX} models the capacitance between the inductor and the substrate. In order to minimize the loss due to R_{sub}, a patterned ground shield may be used that minimizes losses associated with parasitic electric field penetration of the conductive substrate [7]. The parameters of each model element can be extracted through Y-parameters, which can be available through transformation of the S parameters obtained either from EM simulations or from measurement [8].

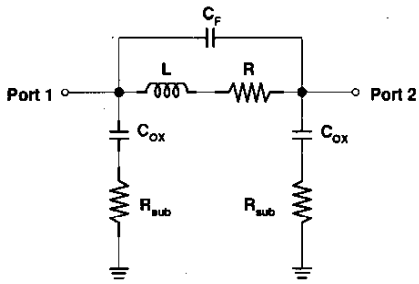


Figure 2. Traditional inductor model.

B. *Modified Hairpin Inductor's Modeling*

For the Hairpin inductor as shown in Figure 1, the coupling capacitance between the turns is very small, so the turn-to-turn coupling capacitance C_F can be ignored. In order to develop a wide-band frequency-independent parameter model, a more complex equivalent circuit, shown in Figure 3, is used to model the hairpin inductor. C_{OX} still models the oxide capacitance between the inductor and the silicon substrate. Csub is added to model the disperssive loss of the substrate versus frequency [9].

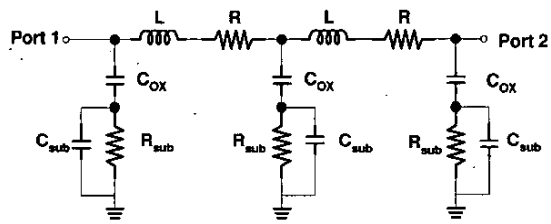


Figure 3. Modified inductor model for the hairpin inductor.

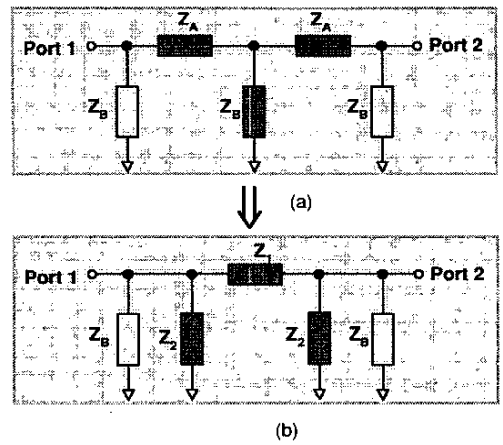
The model extraction methodology is presented as follows. By transforming the complex network (see Figure 3) into a pi-network (see Figure 4(a) and (b)), the parameters become extractable explicitly from the two-port Y parameters by either EM simulations or measurements.

In the first iteration, we simplify the problem by assuming that Z_B, as shown in Figure 4(a), only includes C_{OX} and R_{sub}. The high frequency substrate effects are ignored initially. Thus Z_A and Z_B are given by

$$Z_A = R + j\omega L \tag{2}$$

$$Z_B = R_{sub} + \frac{1}{j\omega C_{OX}} \tag{3}$$

Figure 4. Two-stage pi-circuit to one-stage pi-circuit.



We transform the T network, Z_A-Z_B-Z_A, (see Figure 4 (a)), into a pi-network, Z_2-Z_1-Z_2, (see Figure 4(b)), so that Z_1 and Z_2 can be expressed using two-port Y parameters, which are from either EM simulations or measurements. Then, to solve for Z_A and Z_B from $Z_1(Y)$ and $Z_2(Y)$ equations, one gets:

$$Z_A(Y) = \frac{1 \pm \sqrt{1 + 4\frac{Y_{12} - Y_{11}}{Y_{12}}}}{2(Y_{12} - Y_{11})} \tag{4}$$

and

$$Z_B(Y) = \frac{1 - Y_{12} Z_A(Y)}{Y_{11} + Y_{12}} \tag{5}$$

where, one unreasonable result of Z_A in (4) should be discarded. Then it is not difficult to calculate the model parameter values, R, L, R_{sub} and C_{OX}, from (2), (3), (4) and (5).

Based on (2), R value is extracted from the real part of $Z_A(Y)$. The skin effect and the distributed oxide capacitance still cause small variation on R value. With increasing frequency, the skin effect makes the value rise and the distributed oxide capacitance tends to decrease the value. Generally, the R value (see Table II) can be initially taken at the most interested frequency.

At high frequencies, substrate capacitive effects become more obvious. C_{OX}, calculated from (3) and (5), consists of two components: the oxide capacitance and the substrate capacitance. To achieve a more accurate model, we need to resolve the C_{OX}

into the two parts. More detailed modeling can result in a more frequency-independent model network.

Then, C_{sub} is added back to the Z_B network.. So Z_B is given by

$$Z_{B\_new} = \frac{1}{\frac{1}{R_{sub}} + j\omega C_{sub}} + \frac{1}{j\omega C_{ox}} \quad (6)$$

where we take C_{OX}, calculated from (3) and (5), at a low frequency, as the oxide capacitance part, since at low frequencies, the substrate capacitive effects are negligible. Then the C_{OX} can be obtained:

$$C_{ox} = -\frac{1}{2\pi f \cdot \mathrm{Im}[Z_B(Y)_{\_lowfreq}]} \quad (7)$$

Therefore, we are able to calculate the new R_{sub} and C_{sub} values from (5) and (6).

Finally we have derived all model equations, which are listed in Table I.

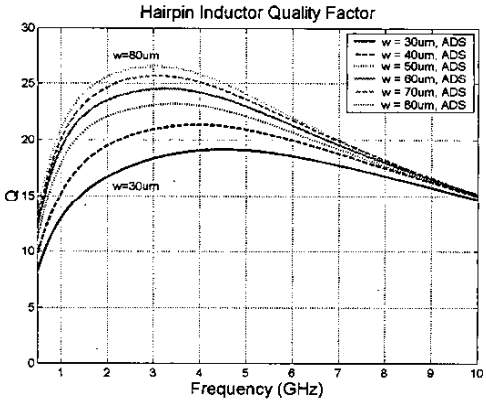
TABLE I
HAIRPIN INDUCTOR MODEL EXPRESSIONS

Model Components in Figure 3	Expressions
R	$R = \mathrm{Re}[Z_A(Y)]$
L	$L = \frac{\mathrm{Im}[Z_A(Y)]}{2\pi f}$
C_{OX}	$C_{OX} = -\frac{1}{2\pi f \cdot \mathrm{Im}[Z_B(Y)_{\_lowfreq}]}$
	$Y_C = \frac{1}{Z_B(Y) - \frac{1}{j\omega C_{OX}}}$
R_{sub}	$R_{sub} = \frac{1}{\mathrm{Re}[Y_C]}$
C_{sub}	$C_{sub} = \frac{\mathrm{Im}[Y_C]}{2\pi f}$

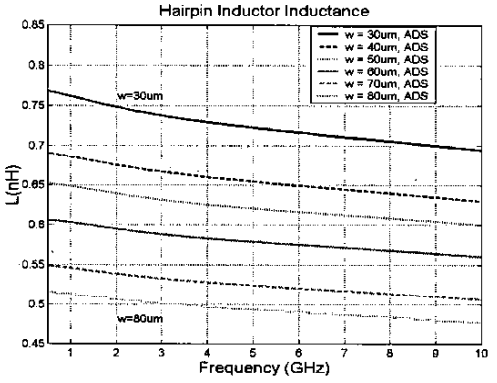
V. MODEL VERIFICATION

A. *Hairpin High Q Performance*

A set of hairpin inductors have been simulated using an EM tool, ADS Momentum [10], and designed in the IBM SiGe BiCMOS process. Simulation data in Figure 5 presents the hairpin inductors' high Q performance and sufficient inductance for RFIC applications, such as VCOs. The examined inductors have length of 1040um and width from 30um, 40um, 50um, 60um, 70um to 80um. Peak Q is varying from 17 to 27 from 3 to 5GHz.



(a) Simulated Quality Factor.



(b) Simulated Inductance.

Figure 5. Hairpin Inductor EM Simulation inductance and quality factor with different metal widths.

B. *Model Parameters for a Hairpin Inductor with 80um Width*

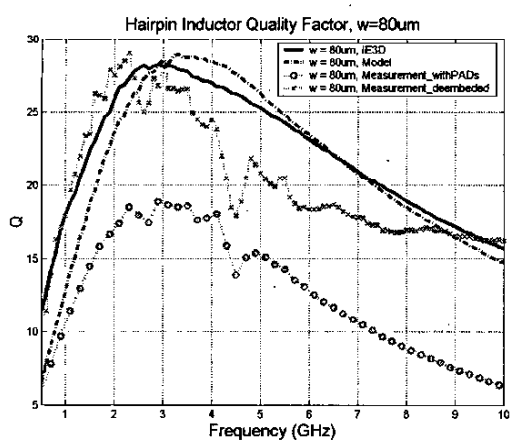
Using the modified modeling approach, presented in last section, a broadband model file has been extracted from the S-parameters of IE3D [11] EM simulations. After optimization, the final model parameters for a hairpin inductor with metal width = 80um and metal length = 1040um are summarized in Table II.

TABLE II
A BROADBAND MODEL FOR A HAIRPIN INDUCTOR WITH W=80um, L= 1040um

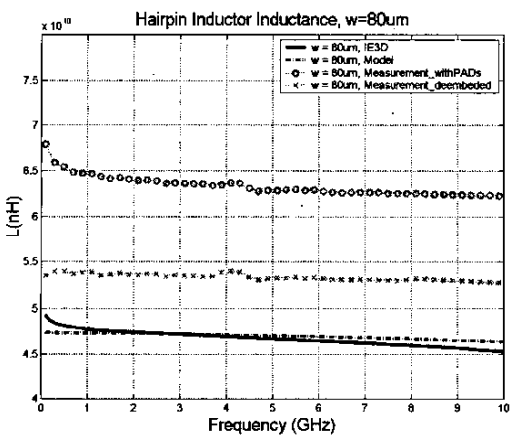
Model Elements in Figure 3	Parameter Values
R	115 mOhm
L	0.237 nH
C_{OX}	125 fF
R_{sub}	300 Ohm
C_{sub}	60 fF

C. *The Model from 1GHz ~ 10GHz vs EM Simulation Comparison*

We have imported the model network (see Table II) in Cadence Analog Environment and compared its performance with the original EM simulation data from IE3D in Figure 6(a) and (b). The hardware measurement data with probe pads are also shown in the figures as references. The probe pads' parasitics (resistance, inductance and capacitance) have been simulated and excluded from the measurement data with pads. After the analytical deembedding, the measured quality factor and inductance are used in the comparison as well. Results in Figure 6(a) and (b) show that the calculated Q and inductance of the derived model network match EM simulations well across the whole frequency range. The measurements show essentially the same values as EM simulations.



(a) Quality factor comparison.



(b) Inductance comparison.

Figure 6. The model verified by EM simulations and referenced by hardware measurement data.

VI. CONCLUSION

A high Q (peak Q of 27) hairpin inductor is designed and fabricated in IBM's 0.5um SiGe BiCMOS technology, the Q of the inductor is increased by optimizing the width of the inductor. An efficient modeling methodology has been presented. A physics-based lumped element model can be extracted from its S-parameter data, which could be obtained from either EM simulations or hardware measurements. The model of an 80um wide hairpin inductor has been developed. The model simulation performance correlates with the original EM simulated data very well.

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